WHAT IS CLAIMED IS

1. A circuit for generating a pixel clock for use in scanning a laser beam, comprising:

a high-frequency-clock generating circuit which generates a high-frequency clock having a higher frequency than the pixel clock; and

a control circuit which generates the pixel clock while shifting a phase of the pixel clock by a shift step proportional to a clock cycle of the high-frequency clock in response to phase data indicative of timing and amounts of phase shifts.

2. The circuit as claimed in claim 1, wherein said control circuit includes:

a phase-synchronizing-signal generating circuit which synchronizes a horizontal synchronizing signal indicative of a start of each

scan with the high-frequency clock for outputting as a phase synchronizing signal;

a transition detecting circuit which detects a transition of the phase synchronizing signal and a transition of the pixel clock, and, in response thereto, generates a detection signal;

a control-signal generating circuit which generates one or more control signals in response to the detection signal and the phase data; and

a pixel-clock controlling circuit which generates the pixel clock while shifting the phase of the pixel clock in response to the one or more control signals.

3. The circuit as claimed in claim 1, wherein said control circuit includes:

a phase-synchronizing-signal generating circuit which receives a horizontal synchronizing signal indicative of a start of each scan, said phase-synchronizing-signal generating circuit synchronizing the horizontal synchronizing signal with a positive transition of the high-frequency

clock for outputting as a first phase synchronizing signal, synchronizing the horizontal synchronizing signal with a negative transition of the high-frequency clock for outputting as a second phase synchronizing signal, and generating a state signal indicative of timing of the horizontal synchronizing signal relative to the high-frequency clock;

a first clock generating circuit which generates a first clock in response to the high-frequency clock, the first phase synchronizing signal, and the phase data;

a second clock generating circuit which generates a second clock in response to the high-frequency clock, the second phase synchronizing signal, and the phase data; and

a selecting circuit which selects one of the first clock and the second clock in response to the state signal for outputting as the pixel clock.

4. The circuit as claimed in claim 1, wherein said control circuit includes:

a phase-synchronizing-signal generating

circuit which receives a horizontal synchronizing signal indicative of a start of each scan, said phase-synchronizing-signal generating circuit synchronizing the horizontal synchronizing signal with a positive transition of the high-frequency clock for outputting as a first phase synchronizing signal, synchronizing the horizontal synchronizing signal with a negative transition of the high-frequency clock for outputting as a second phase synchronizing signal, and generating a state signal indicative of timing of the horizontal synchronizing signal relative to the high-frequency clock;

a first clock generating circuit which generates a first clock in response to the high-frequency clock, the first phase synchronizing signal, and the phase data;

a second clock generating circuit which generates a second clock in response to the high-frequency clock, the second phase synchronizing signal, and the phase data; and

a selecting circuit which selects one of the first clock and the second clock in response to the state signal and the phase data for outputting as the pixel clock.

5. The circuit as claimed in claim 1, wherein said control circuit includes:

a phase-synchronizing-signal generating circuit which synchronizes a horizontal synchronizing signal indicative of a start of each scan with a plurality of different transition timings of the high-frequency clock to generate a plurality of respective phase synchronizing signals, one of which is selected for outputting as a phase synchronizing signal;

a transition detecting circuit which detects a transition of the phase synchronizing signal and a transition of the pixel clock, and, in response thereto, generates a detection signal;

a control-signal generating circuit which generates one or more control signals in response to the detection signal and the phase data; and

a pixel-clock controlling circuit which generates the pixel clock while shifting the phase of the pixel clock in response to the one or more control signals.

6. The circuit as claimed in claim 1, wherein said control circuit includes:

a phase-synchronizing-signal generating circuit which receives a horizontal synchronizing signal indicative of a start of each scan, said phase-synchronizing-signal generating circuit synchronizing the horizontal synchronizing signal with a plurality of different positive transitions of the high-frequency clock to generate a plurality of respective phase synchronization signals, one of which is selected for outputting as a first phase synchronizing signal, synchronizing the horizontal synchronizing signal with a plurality of different negative transitions of the high-frequency clock to generate a plurality of respective phase synchronization signals, one of which is selected for outputting as a second phase synchronizing signal, and generating a state signal indicative of timing of the horizontal synchronizing signal relative to the high-frequency clock;

a first clock generating circuit which generates a first clock in response to the high-

frequency clock, the first phase synchronizing signal, and the phase data;

a second clock generating circuit which generates a second clock in response to the high-frequency clock, the second phase synchronizing signal, and the phase data; and

a selecting circuit which selects one of the first clock and the second clock in response to the state signal for outputting as the pixel clock.

7. The circuit as claimed in claim 1, wherein said control circuit includes:

a phase-synchronizing-signal generating circuit which receives a horizontal synchronizing signal indicative of a start of each scan, said phase-synchronizing-signal generating circuit synchronizing the horizontal synchronizing signal with a plurality of different positive transitions of the high-frequency clock to generate a plurality of respective phase synchronization signals, one of which is selected for outputting as a first phase synchronizing signal, synchronizing the horizontal

synchronizing signal with a plurality of different negative transitions of the high-frequency clock to generate a plurality of respective phase synchronization signals, one of which is selected for outputting as a second phase synchronizing signal, and generating a state signal indicative of timing of the horizontal synchronizing signal relative to the high-frequency clock;

a first clock generating circuit which generates a first clock in response to the high-frequency clock, the first phase synchronizing signal, and the phase data;

a second clock generating circuit which generates a second clock in response to the high-frequency clock, the second phase synchronizing signal, and the phase data; and

a selecting circuit which selects one of the first clock and the second clock in response to the state signal and the phase data for outputting as the pixel clock.

8. A method of generating a pixel clock

for use in scanning a laser beam, comprising the steps of:

generating a high-frequency clock having a higher frequency than the pixel clock; and

generating the pixel clock while shifting a phase of the pixel clock by a shift step proportional to a clock cycle of the high-frequency clock in response to phase data indicative of timing and amounts of phase shifts.

9. The method as claimed in claim 8, wherein said step of generating the pixel clock includes the steps of:

synchronizing a horizontal synchronizing signal indicative of a start of each scan with the high-frequency clock for providing as a phase synchronizing signal;

detecting a transition of the phase synchronizing signal and a transition of the pixel clock to generate a detection signal;

generating one or more control signals in response to the detection signal and the phase data;

and

generating the pixel clock while shifting the phase of the pixel clock in response to the one or more control signals.

10. The method as claimed in claim 8, wherein said step of generating the pixel clock includes the steps of:

receiving a horizontal synchronizing signal indicative of a start of each scan;

synchronizing the horizontal synchronizing signal with a positive transition of the high-frequency clock for providing as a first phase synchronizing signal;

synchronizing the horizontal synchronizing signal with a negative transition of the high-frequency clock for providing as a second phase synchronizing signal;

generating a state signal indicative of timing of the horizontal synchronizing signal relative to the high-frequency clock;

generating a first clock in response to

the high-frequency clock, the first phase synchronizing signal, and the phase data;

generating a second clock in response to the high-frequency clock, the second phase synchronizing signal, and the phase data; and

selecting one of the first clock and the second clock in response to the state signal for outputting as the pixel clock.

11. The method as claimed in claim 8, wherein said step of generating the pixel clock includes the steps of:

receiving a horizontal synchronizing signal indicative of a start of each scan;

synchronizing the horizontal synchronizing signal with a positive transition of the high-frequency clock for providing as a first phase synchronizing signal;

synchronizing the horizontal synchronizing signal with a negative transition of the high-frequency clock for providing as a second phase synchronizing signal;

generating a state signal indicative of timing of the horizontal synchronizing signal relative to the high-frequency clock;

generating a first clock in response to the high-frequency clock, the first phase synchronizing signal, and the phase data;

generating a second clock in response to the high-frequency clock, the second phase synchronizing signal, and the phase data; and

selecting one of the first clock and the second clock in response to the state signal and the phase data for outputting as the pixel clock.

12. An image forming apparatus, comprising:

a pixel-clock generating unit which generates a pixel clock;

a laser drive unit which emits a laser beam in response to the pixel clock and image data;

a photoconductor; and

a deflector which scans the laser beam on said photoconductor to form an image on said

photoconductor, wherein said pixel-clock generating unit includes:

a high-frequency-clock generating circuit which generates a high-frequency clock having a higher frequency than the pixel clock; and

a control circuit which generates the pixel clock while shifting a phase of the pixel clock by a shift step proportional to a clock cycle of the high-frequency clock in response to phase data indicative of timing and amounts of phase shifts.

13. The image forming apparatus as claimed in claim 12, further comprising:

photo-detectors which detect the laser beam; and

a dot-position-error detecting and controlling unit which measures a time length of each scan of the laser beam in response to signals from said photo-detectors, and corrects the phase data in response to the measured time length.